Amendments to the Specification:

Please amend paragraph number **[0022]** as follows:

[0022] The term "semiconductor wafer" as used herein means and includes a bulk substrate comprised of any of various semiconductive materials including, but not limited to, silicon, silicon-on-~~saphire~~sapphire (SOS), silicon-on-insulator (SOI), silicon-on-glass (SOG), galium arsenide, iridium phosphide, etc.

Please amend paragraph number **[0029]** as follows:

[0029] Adjacent die interconnection circuit 50 is formed on a surface 52 of the passivation layer 46 and may be used to interconnect any external connection such as conductive bumps 42, 43 with the bond pads 40, 41. The adjacent die interconnection circuit 50 includes conductor segment 54 in electrical communication with bond pad 40 and extending away therefrom to bond pad 41 of functional die 20, and an outer passivation layer 56 which covers the conductor segment 54. The outer passivation layer 56 of the adjacent die interconnection circuit 50 insulates the conductor segment 54, and apertures may be formed therethrough to locate and facilitate the formation of conductive ~~bump~~ bumps 42, 43. Both passivation layer 46 and outer passivation layer 56 may comprise a dielectric material, with suitable materials for outer passivation layer 56 including polymers such as polyimide, glasses such as PSG, BSG or BPSG, or oxides, such as SiO_2.